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Description

SWITCHED CAPACITOR CIRCUIT CAPABLE OF MINIMIZING CLOCK FEEDTHROUGH EFFECT IN A VOLTAGE CONTROLLED OSCILLATOR CIRCUIT

Cross Reference To Related Applications

[0001] This is a continuation-in-part of U.S. Application No. 10/250,082, filed 03 June, 2003, and which is included herein by reference.

Background of Invention

[0002] 1. Field of the Invention

[0003] The present invention relates to a switched capacitor circuit, and more particularly, to a switched capacitor circuit used in a voltage controlled oscillator (VCO) that can minimize the clock feedthrough effect thereby preventing a VCO frequency drift phenomenon during calibration and the synthesizer phase locking period.

[0004] 2. Description of the Prior Art

[0005] A voltage controlled oscillator (VCO) is commonly used for frequency synthesis in wireless communication circuits. As Welland, et al. state in US Patent 6,226,506, wireless communication systems typically require frequency synthesis in both the receive path circuitry and the transmit path circuitry.

[0006] Fig.1 shows a VCO circuit according to the prior art. An LC type VCO 10 used in a frequency synthesizer contains aresonator, and the basic resonant structure includes an inductor 12 connected between a first oscillator node OSC_P and a second oscillator node OSC_N. Connected in parallel with the inductor 12 is a continuously variable capacitor 14 and a plurality of discretely variable capacitors 16. The continuously variable capacitor 14 is used for fine-tuning a desired capacitance while the plurality of discretely variable capacitors 16 is used for coarse tuning. The resistive loss of the parallel combination of inductor and capacitors is compensated by a negative resistance generator 18 to sustain the oscillation.

[0007] Each discretely variable capacitor in the plurality of discretely variable capacitors 16 is made up of a switched capacitor circuit 20 and each switched capacitor circuit is controlled by an independent control signal (SW_1 to

SW_N). Based on the control signal SW_N the switched capacitor circuit 20 can selectively connect or disconnect a capacitor 24 to the resonator of the VCO 10. Different on/off combinations of switched capacitor arrays results in a wider capacitance range of the LC type resonator and hence a wider VCO 10 oscillation frequency coverage.

[0008] Fig.2 shows a switched capacitor circuit 20a according to the prior art. A capacitor 30 is connected between the first oscillator node OSC_P and a node A. A switch element 32 selectively connects node A to ground, and the switch element 32 is controlled by a control signal SW. When the switch element 32 is turned on, the capacitance associated with the capacitor 30 is added to the overallcapacitance in the VCO 10 resonator. When the switch element 32 is turned off, the capacitance looking into the first oscillator node OSC_P is the series combination of the capacitor 30 and the off state capacitance associated with the switch element 32.

[0009] Fig.3 shows a differential type switched capacitor circuit 20b according to the prior art. Differential implementations have much greater common-mode noise rejection and are widely used in high-speed integrated circuit environments. In the differential switched capacitor circuit

20b, a positive side capacitor 40 is connected between the first oscillator node OSC_P and a node A. A positive side switch element 42 selectively connects node A to ground. A negative side capacitor 44 is connected between the second oscillator node OSC_N and a node B. A negative side switch element 46 selectively connects node B to ground. The two switch elements 42, 46 are controlled by the same control signal SW. When the switch elements 42, 46 are turned on, the capacitance associated with the series combination of the positive and negative side capacitors 40, 44 is added to the overall capacitance in the VCO 10. When the switch elements 42, 46 are turned off, the differential input capacitance is the series combination of the positive and negative side capacitors 40, 44 and other switch parasitic capacitance. The overall input capacitance when all switch elements 42, 46 are turned off is lower than that when all switch elements 42, 46 are turned on.

[0010] Fig.4 shows a second differential type switched capacitor circuit 20c according to the prior art. The second differential switched capacitor circuit 20c is comprised of the same components as the first differential switched capacitor circuit 20c and there is also a center switch element 48 used to lower the overall turn-on switch resistance

connected betweennode A and node B. All three switch elements 42, 46, 48 are controlled by the same control signal SW. When the switch elements 42, 46, 48 are turned on, the capacitance associated with the series combination of the positive and negative side capacitors 40, 44 is added to the overall capacitance in the VCO 10. When the switch elements 42, 46, 48 are turned off, the differential input capacitance is the series combination of the positive and negative side capacitors 40, 44 and other switch parasitic capacitance. The overall input capacitance when all switch elements 42, 46, 48 are turned off is lower than that when all switch elements 42, 46, 48 are turned on.

[0011] Regardless of whether the single ended implementation shown in Fig.2 or one of the differential implementations shown in Fig.3 and Fig.4 is used, when the switched capacitor circuit 20a, 20b, 20c is turned off, a momentary voltage step change occurs at node A (and in the case of the differential implementations also at node B). The momentary voltage step causes an undesired change in the overall capacitance, and ultimately, an undesired change in the VCO 10 frequency. Because NMOS switches are used in the examples shown in Fig.2, Fig.3, and Fig.4, the momentary voltage step change is a voltage drop when

the switch elements 32, 42, 46, 48 are turned off.

[0012] Using the single ended case shown in Fig.2 as an example, when the switch element 32 is turned off, charge carriers are injected to the junction capacitance connected between the first terminal and the second terminal of the switch element 32. The injection produces an undesired voltage step change across the capacitive impedance and appears as a voltage drop at node A. This effect is known as clock feedthrough effect and appears as a feedthrough of the control signal SW from the control terminal of the switch element 32 to the first and second terminals of the switch element 32. When the switch element 32 is turned on, node A is connected to ground so the feedthrough of the control signal SW is of no consequence. However, when the switch element 32 is turned off, the feedthrough of the control signal SW causes a voltage step, in the form a voltage drop to appear at node A. Because of the dropped voltage at node A, the diode formed by the N^+ diffusion of switch element 32 and the P type substrate in the off state will be slightly forward biased. The voltage level at node A will spike low and then recover to ground potential as the slightly forward biased junction diode formed by the switch element 32 in the off state allows

subthreshold and leakage currents to flow. The voltage drop and recovery at node A changes the loaded capacitance of the VCO 10 resonator and causes an undesired momentarily drift in the VCO 10 frequency.

[0013] When the differential switched capacitor circuit 20c shown in Fig.4 switches off, it suffers from the same clock feedthrough effect problem at node A and at node B. The positive side node A has an undesired voltage step change caused by the clock feedthrough effect of both the positive side switch element 42 and the clock feedthrough effect of the center switch element 48. Similarly, the negative side node B has an undesired voltage step change caused by the clock feedthrough effect of both the negative side switch element 46 and the clock feedthrough effect of the center switch element 48. The voltage step change and recovery at node A and node B changes the loaded capacitance of the VCO 10 resonator and causes an undesired momentary drift in the VCO 10 frequency.

SUMMARY OF INVENTION

[0014] It is therefore a primary objective of the present invention to provide a switched capacitor circuit capable of minimizing the clock feedthrough effect, to solve the above-mentioned problem.

[0015] According to the present invention, a switched capacitor circuit capable of minimizing clock feedthrough effect is disclosed. The switched capacitor circuit comprises a first positive side switch element for selectively connecting a first positive side node to a third node depending upon a first control signal, wherein the first positive side node is connected to a positive side capacitor. A second positive side switch element is for selectively connecting the first positive side node to a second node depending upon a second control signal, and a third switch element is for selectively connecting the third node to the second node depending upon a third control signal. A sequence controller connected to the switch elements generates the first control signal, the second control signal, and the third control signal.

[0016] According to the present invention, a method is disclosed for minimizing clock feedthrough effect when switching off a switched capacitor circuit. The method comprises the following steps: (a) Disconnecting a first positive side node from a third node through a first positive side switch element. (b) Disconnecting the first positive side node from a second node through a second positive switch element. (c) Disconnecting the third node from the second

node through a third positive side switch element. Wherein, the first positive side node is connected to a positive side capacitor and the sequence of steps (b) and (c) are interchangeable.

[0017] It is an advantage of the present invention that by switching off the switch elements sequentially in an order of decreasing size, the switched capacitor circuit is gradually switched off to minimize the clock feedthrough effect and therefore the undesired drift of the VCO 10 frequency.

[0018] It is a further advantage of the present invention that by using a third switch element to isolate the largest switch elements from a ground or power node, the subthreshold and leakage currents passing through the largest switch elements once they are switched off are blocked and the VCO 10 stabilizes to a steady state frequency at a much lower rate.

[0019] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0020] Fig.1 is a schematic diagram of a typical Voltage Con-

trolled Oscillator (VCO) circuit used in a frequency synthesizer according to the prior art.

[0021] Fig.2 is a switched capacitor circuit used in the VCO of Fig.1 according to the prior art.

[0022] Fig.3 is a differential type switched capacitor circuit used in the VCO of Fig.1 according to the prior art.

[0023] Fig.4 is the differential type switched capacitor circuit of Fig.3 with the addition of a center switch element.

[0024] Fig.5 is a first embodiment switched capacitor circuit according to the present invention.

[0025] Fig.6 is a first time domain plot of the control signals generated by the sequence controller of Fig.5.

[0026] Fig.7 is a second time domain plot of the control signals generated by the sequence controller of Fig.5.

[0027] Fig.8 is a third time domain plot of the control signals generated by the sequence controller of Fig.5.

[0028] Fig.9 is a second embodiment switched capacitor circuit according to the present invention.

[0029] Fig.10 is a time domain plot of the control signals generated by the sequence controller of Fig.9.

[0030] Fig.11 is a third embodiment differential type switched capacitor circuit 20f according to the present invention.

[0031] Fig.12 is a time domain plot of the control signals gener-

ated by the sequence controller of Fig.11.

[0032] Fig.13 is a fourth embodiment differential type switched capacitor circuit according to the present invention.

[0033] Fig.14 is a time domain plot of the control signals generated by the sequence controller of Fig.13.

DETAILED DESCRIPTION

[0034] Fig.5 shows a first embodiment switched capacitor circuit 20d according to the present invention. In Fig.5, the switched capacitor circuit 20d comprises a capacitor 50, a first switch element 52, a second switch element 54, a third switch element 56, and a sequence controller 58. In the first embodiment, the switch elements are NMOS transistors, the first switch element 52 being larger than the second switch element 54, and the second switch element 54 being larger than the third switch element 56. The capacitor 50 is connected between the first oscillator node OSC_P and a node A. The first switch element 52 selectively connects node A to node C depending on a first control signal SW1. The second switch element 54 selectively connects node A to the second oscillator node OSC_N, which is connected to ground, depending on a second control signal SW2. The third switch element 56 selectively connects node C to the second oscillator node

OSC_N depending on a third control signal SW3. The sequence controller 58 generates the first, second, and third control signals SW1, SW2, SW3. As an alternative embodiment, the switch elements can be implemented as PMOS transistors, wherein the oscillator node OSC_N is a VCC power supply node. For this alternative embodiment, the polarity of control signals is reversed.

[0035] Fig.6 shows a first time domain plot 60 of the control signals generated by the sequence controller 58. In order to gradually switch the switched capacitor circuit 20d to an off state, the sequence controller 58 ensures that the switch elements 52, 54, 56 are switched off in decreasing order based on switch size. Because the first switch element 52 is larger than the second switch element 54, the first switch element 52 is first switched off at time t_1. Because the second switch element 54 is larger than the third switch element 56, the second switch element 54 is next switched off at time t_2. Finally, at time t_3, the third switch element 56 is switched off. Since the amount of voltage change at node A due to the clock feedthrough effect depends on the parasitic capacitance ratio of control terminal (gate) to first terminal (drain) and first terminal to second terminal (source) capacitance, the smaller

the control terminal to first terminal capacitance, the smaller the voltage change due to the feedthrough of the control signal switching from high to low. The present invention takes advantage of this fact because the larger switch element 52 with a larger voltage drop due to the clock feedthrough effect is switched off first. Until the second switch element 54 is switched off, node A is connected to ground and the clock feedthrough effect due to the first switch element 52 is not a concern. If the second switch element 54 is made sufficiently small, the clock feedthrough effect for this switch changing from the on to off state can be made negligible.

[0036] However, when the second switch element 54 is switched off, node A still experiences a slightly negative voltage drop due to the clock feedthrough effect. Because of the existence of subtheshold and leakage currents through the switch elements 52, 54, 56, the node A potential eventually returns to ground. The larger the switch element, the larger the subtheshold and leakage currents. The purpose of the third switch element 56 is to isolate the first switch element 52, which is the largest switch element, from ground to delay the node A returning to ground potential. By delaying the voltage at node A return

to ground potential during the synthesizer phase locking period, node A remains at a slightly negative but constant voltage potential for a longer period of time. The frequency synthesizer can therefore lock the VCO 10 frequency faster.

[0037] Fig.7 shows a second time domain plot 70 of the control signals generated by the sequence controller 58. In order to gradually switch the switched capacitor circuit 20d to an off state, the sequence controller 58 ensures that the first switch element 52 is switched off first at time t_1.The third switch element 56 is shut off at the same time as the second switch element 54 at time t_2.

[0038] Fig.8 shows a third time domain plot 80 of the control signals generated by the sequence controller 58. In order to gradually switch the switched capacitor circuit 20d to an off state, the sequence controller 58 again ensures that the first switch element 52 is switched off first at time t_1. However, to further prevent subtheshold and leakage currents from passing through the first switch element 52 when node A is not connected to ground, the third switch element 56 is switched off next at time t_2. After the first switch element 52 has been disconnected from ground by the third switch element 56, the second switch element 54

is switched off at time t_3.

[0039] Fig.9 shows a second embodiment switched capacitor circuit 20e according to the present invention. Fig.9 comprises the same components as the first embodiment switched capacitor circuit 20d shown in Fig.5 with the addition of a low-pass filter 90 for making the second and third switch elements 54, 56 gradually switch off. The first switch element 52 is controlled by the first control signal SW1, while the second and third switch elements 54, 56 are both controlled by the output of the low-pass filter 90 (SW2_filter), which is a low-pass filtered version of the second control signal SW2. It should also be noted that, in Fig.5, a low pass filter could also be added at the second and/or third switch control signals, SW2 and SW3.

[0040] Fig.10 shows a time domain plot 100 of the control signals generated by the sequence controller 58. In order to gradually switch the switched capacitor circuit 20e to an off state, the sequence controller 58 ensures that the first switch element 52 is switched off first at time t_1. The low-pass filter 90 causes the signal SW2_filter, used to control the second and third switch elements 54, 56, to gradually change from a logic high to a logic low and in this way minimize the voltage step change seen at node A. Because

the second switch element 54 is gradually switched off, node A is gradually disconnected from ground. As the second switch element 54 is gradually switched off, during a period of delay time there exists a conduction path of the switch element 54, with an increasing resistance as time advances, to ground to minimize the clock feedthrough effect. In contrast to the prior art, the present invention does not forward bias the parasitic diode formed by the switch element 54 in the off state. The clock feedthrough effect at each moment of time is reduced. As shown in Fig.9, the third switch element is also controlled by the output of the low-pass filter 90 (SW2_filter) to minimize the clock feedthrough effect of the third switch element itself. It should also be noted that the third switch element could also be directly controlled by the second control signal SW2 and does not necessarily need to have its control signal low-pass filtered.

[0041] Fig.11 shows a third embodiment differential type switched capacitor circuit 20f according to the present invention. In Fig.11, the switched capacitor circuit 20f comprises a positive side capacitor 110, a negative side capacitor 112, a first positive side switch element 114, a first negative side switch element 116, a second positive

side switch element 118, a second negative side switch element 120, a third switch element 122, a center switch element 126, and a sequence controller 124. In the third embodiment, the switch elements are NMOS transistors, the first positive side switch element 114 and the first negative side switch element 116 being of substantially the same size and larger than the second positive side switch element 118 and the second negative side switch element 120, which are also of substantially the same size. Additionally, the third switch element 122 is substantially the same size as the second positive and negative side switch elements 118, 120. The positive side capacitor 110 is connected between the first oscillator node OSC_P and a node A. The negative side capacitor 112 is connected between the second oscillator node OSC_N and a node B. The center switch element 126 selectively connects node A to node B depending on a center control signal SW_center. The first positive side switch element 114 selectively connects node A to node C depending on a first control signal SW1. The first negative side switch element 116 selectively connects node B to node C depending on the first control signal SW1. The second positive side switch element 118 selectively connects node A to

ground depending on the second control signal SW2, and the second negative side switch element 120 selectively connects node B to ground depending on the second control signal SW2. The third switch element 122 selectively connects node C to ground depending on a third control signal SW3. Finally, the sequence controller 124 generates the first, second, and third control signals SW1, SW2, SW3 as well as the center control signal SW_center.

[0042] Fig.12 shows a time domain plot 128 of the control signals generated by the sequence controller 124. In order to gradually switch the switched capacitor circuit 20f to an off state, the sequence controller 124 ensures that the center switch element 126 is switched off first at time t_1. The first positive and negative switch elements 114, 116 are switched off next at time t_2.To further prevent any subtheshold and leakage currents from passing through the first positive and negative side switch elements 114, 116 when node A and node B is not connected to ground, the third switch element 122 is switched off next at time t_3. After the first positive and negative side switch elements 114, 116 have been disconnected from ground by the third switch element 122, the second positive and negative side switch elements 118, 120 are switched off

at time t_4. It should be noted that although Fig.11 includes the center switch element 126 and the sequence controller 124 generates the center control signal SW_center, the center switch element is an optional component used to lower the overall turn-on switch resistance. Without the center switch element 126, the switched capacitor circuit 20f is itself another embodiment of the differential type switched capacitor circuit.

[0043] Additionally, there are three different combinations for the turn off timing t_3 and t_4 for the second and third positive/negative side switch elements. Time t_3 can lead, lag or be equal to the time t_4. For each combination, a low pass filter can be added at the switch control signals SW2 and SW3 to minimize the clock feedthrough effect caused by the corresponding switches themselves.

[0044] Fig.13 shows a fourth embodiment differential type switched capacitor circuit 20g according to the present invention. In Fig.13, the switched capacitor circuit 20g comprises a positive side capacitor 130, a negative side capacitor 132, a first positive side switch element 134, a first negative side switch element 136, a second positive side switch element 138, a second negative side switch element 140, a third switch element 142, a center switch

element 146, a low-pass filter 148, and a sequence controller 144. In the fourth embodiment, the switchelements are PMOS transistors, the first positive side switch element 134 and the first negative side switch element 136 being of substantially the same size and larger than the second positive side switch element 138 and the second negative side switch element 140, which are also of substantially the same size. Additionally, the third switch element 142 is of substantially the same size as the second positive and negative side switch elements 138, 140. The sequence controller 144 generates a center control signal SW_center, a first control signal SW1, and a second control signal SW2. The second control signal is connected to the input of the low-pass filter 148 and the output of the low-pass filter is a filtered version of the second control signal SW2_filter. The positive side capacitor 130 is connected between the first oscillator node OSC_P and a node A. The negative side capacitor 132 is connected between the second oscillator node OSC_N and a node B. The center switch element 146 selectively connects node A to node B depending on a center control signal SW_center. The first positive side switch element 134 selectively connects node A to node C depending on a first control signal

SW1. The first negative side switch element 136 selectively connects node B to node C depending on the first control signal SW1. The second positive side switch element 138 selectively connects node A to a VCC power supply node depending on the filtered control signal SW_filter, and the second negative side switch element 140 selectively connects node B to the VCC power supply node depending on the filtered control signal SW_filter. Finally, the third switch element 142 selectively connects node C to the VCC power supply node depending on the filtered control signal SW_fitler.

[0045] Like the NMOS-based switch of Fig.11, the sequence controller can also generate 4 control signals for: the center switch element 146, the first positive/negative side switch elements, the second positive/negative side switch elements, and the third switch element. The second positive/negative side switch elements and the third switch element can have the aforementioned turn off timing combinations and can further include a low pass filter connected to the control signals to minimize the clock feedthrough effect.

[0046] Fig.14 shows a time domain plot 150 of the control signals generated by the sequence controller 144. In order to

gradually switch the switched capacitor circuit 20g to an off state, the sequence controller 144 ensures that the center switch element 146 is switched off first at time t_1. The first positive and negative switch elements 134, 136 are switched off next at time t_2.To prevent any subthesh-old and leakage currents from passing through the first positive and negative side switch elements 134, 136 when node A and node B are not connected to ground, the third switch element 142, and the second positive and negative side switch elements 138, 140 are switched off next at time t_3 using the filtered control signal SW2_filter. It should be noted that although Fig.13 includes the center switch element 146 and the sequence controller 144 gen-erates the center control signal SW_center, the center switch element is an optional component used to lower the overall turn-on switch resistance of the switched ca-pacitor circuit 20g. Without the center switch element 146, the switched capacitor circuit 20g is itself another embodiment of the differential type switched capacitor circuit.

[0047] In contrast to the prior art, the present invention gradually switches off the switched capacitor circuit so that the clock feedthrough effect is minimized and accordingly the

undesired frequency drift of the VCO 10 frequency is properly reduced. When switching off, the prior art implementations suffer from clock feedthrough effect that causes a voltage step change to occur at an internal capacitive node of the VCO 10 resonator. The voltage step change causes the junction diode formed by a switch element in the off state to be slightly forward biased until the dropped voltage returns to the ground potential. According to the present invention, the voltage step change at the internal capacitive node is minimized. When switching off, the present invention minimizes the momentary change of the capacitance value of the VCO 10 resonator and the momentary drift in the VCO 10 frequency. Additionally, the subtheshold and leakage currents passing through the largest switch elements are blocked by the use of an additional switch element. The additional switch element effectively isolates the largest switch element having the largest subtheshold and leakage currents from a ground or power supply node. This further stabilizes the voltage change at node A during the synthesizer locking period, allowing the VCO 10 frequency to be locked faster than the prior art.

[0048] Those skilled in the art will readily observe that numerous

modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, that above disclosure should be construed as limited only by the metes and bounds of the appended claims.